## **CLAIMS**

## What is claimed is:

- 1. A method for testing a device-under-test (DUT), the method comprising the steps of: 1 examining a test data file that includes test data configured to enable testing the 2 DUT, the test data file including a first plurality of data units and a second 3 plurality of data units, the first plurality of data units corresponding to a first 4 plurality of DUT pins, and the second plurality of data units corresponding to 5 a second plurality of DUT pins; and 6 separating the first plurality of data units from the second plurality of data units, 7 wherein the first plurality of data units are communicated to the first plurality 8 of DUT pins and the second plurality of data units are communicated to the 9 second plurality of DUT pins. 10
- 1 2. The method of claim 1, wherein the first plurality of data units have at least one
- 2 different property than the second plurality of data units.
- 1 3. The method of claim 2, wherein the at least one different property includes timing
- 2 complexity.
- 4. The method of claim 2, wherein the at least one different property includes vector data
- 2 volume.
- 1 5. The method of claim 2, wherein the at least one different property includes repetitive
- 2 data patterns.
- 1 6. The method of claim 1, wherein the first plurality of DUT pins are scan-pins and the
- 2 second plurality of DUT pins are non-scan pins.
- 1 7. The method of claim 1, further comprising the step of:

formatting the first plurality of data units independently from the second plurality 2 of data units. 3 8. The method of claim 1, wherein the test data file is one of a STIL (standard test 1 interface language) file and a WGL (waveform generation language) file. 2 9. The method of claim 1, wherein at least one processor operating in a first timing 1 domain enables the first plurality of data units to be provided to the first plurality of DUT 2 pins, and at least one processor operating in a second timing domain enables second 3 plurality of data units to be provided to the second plurality of DUT pins, wherein the 4 second timing domain is different from the first timing domain. 5 10. A method for testing a device-under-test (DUT), the method comprising the steps of: 1 examining a test data file that includes test data configured to enable testing the 2 DUT, the test data file including a first plurality of data units and a second 3 plurality of data units, the first plurality of data units corresponding to a first 4 plurality of DUT pins, and the second plurality of data units corresponding to 5 a second plurality of DUT pins; and 6 identifying the first plurality of DUT pins; and 7 storing information identifying first plurality of DUT pins in memory. 8 11. The method of claim 10, further comprising the step of: 1 providing the information to a module configured to format the test data file. 2 12. The method of claim 10, further comprising the step of: 1 formatting the first plurality of data units independently from the second plurality 2 of data units. 3 13. The method of claim 10, wherein the first plurality of DUT pins are scan-pins and the 1 second plurality of DUT pins are non-scan pins. 2

14. The method of claim 10, wherein the test data file is one of a STIL (standard test 1 interface language) file and a WGL (waveform generation language) file. 2 15. The method of claim 10, wherein the first plurality of data units have at least one 1 different property than the second plurality of data units. 2 16. A system for testing a device-under-test (DUT), the system comprising: 1 memory operative to store a test data file that includes test data configured to enable 2 testing the DUT, the test data file including a first plurality of data units and 3 a second plurality of data units, the first plurality of data units corresponding 4 to a first plurality of DUT pins, and the second plurality of data units 5 corresponding to a second plurality of DUT pins; and 6 a processor that is programmed to separate the first plurality of data units from the 7 second plurality of data units. 8 17. The system of claim 16, wherein the processor is programmed to provide the first 1 plurality of data units and the second plurality of data units to a device configured to format 2 the first plurality of data units independently from the second plurality of data units. 3 4 18. The system of claim 16, wherein the first plurality of DUT pins are scan-pins and the 1 second plurality of DUT pins are non-scan pins. 2 19. A system for testing a device-under-test (DUT), the system comprising: 1 memory operative to store a test data file that includes test data configured to enable 2 testing the DUT, the test data file including a first plurality of data units and 3 a second plurality of data units, the first plurality of data units corresponding 4 to a first plurality of DUT pins, and the second plurality of data units 5 corresponding to a second plurality of DUT pins; and 6

7	a processor that is programmed to identify the first plurality of DUT pins based on
8	information contained in the test data file, and to store information
9	identifying the first plurality of DUT pins in memory.
1	20. The system of claim 19, wherein the processor is programmed to provide the
2	information identifying the first plurality of DUT pins to a device configured to format
3	test data.
4	
1	21. The system of claim 19, wherein the first plurality of DUT pins are scan-pins and the
2	second plurality of DUT pins are non-scan pins.
1	22. A system for testing a device-under-test (DUT), the system comprising:
2	means operative to store a test data file that includes test data configured to enable
3	testing the DUT, the test data file including a first plurality of data units and
4	a second plurality of data units, the first plurality of data units corresponding
5	to a first plurality of DUT pins, and the second plurality of data units
6	corresponding to a second plurality of DUT pins; and
7	means operative to identify the first plurality of DUT pins based on information
8	contained in the test data file.